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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

In re Application of:
KNIGHT et al.

Serial No.: 08/082,328

Group Art Unit: 2835

Filed: June 24, 1993

Examiner: J. Vigushin

For: METHOD AND APPARATUS FOR
NON-CONDUCTIVELY
INTERCONNECTING INTEGRATED
CIRCUITS

Attorney Docket No.: 7828-001999

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BRIEF ON APPEAL

Assistant Commissioner for Patents
BOX AF
Washington, D.C. 20231

Sirs:

(1) Real Party in Interest

The present application is assigned to Polychip, a Massachusetts corporation, which is the real party in interest.

(2) Related Appeals and Interferences

There are no related appeals or interferences.

(3) Status of Claims

At filing, 205 claims were submitted.

Claims 29, 80-101 and 201-202 were canceled on June 14, 1995, in a response to a restriction requirement.

Claims 206-209 were added by an amendment mailed on September 9, 1996.

Claims 2-27, 30-36, 49-51, 60-79, 103-142, 145, 148-200 and 203-209 were withdrawn from consideration in an Office Action mailed August 25, 1997.

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As a result, claims 1, 28, 37-48, 52-59, 102, 143, 144, 146 and 147 remain under prosecution. Of these claims, claims 44 and 59 have been allowed.

The remaining claims under prosecution, namely claims 1, 28, 37-43, 45-48, 52-58, 102, 143, 144, 146 and 147 are the subject of this appeal.

Claim 1 has been rejected under 35 U.S.C. 102(b) as anticipated by Hite (USP 5,103,283), Dehaine et al. (USP 4,982,311) and Tanaka (JP 63-15435A).

Claim 1 and the other pending claims except claims 44 and 59 have been rejected under 35 U.S.C. 102(e) as anticipated by, or in the alternative under 35 U.S.C. 103(a) as obvious over Moresco et al. (USP 5,404,265).

(4) Status of Amendments

No amendments were filed subsequent to the final rejection.

(5) Summary of the Invention

Applicant's claimed invention relates to an apparatus for communicating or signalling between integrated circuit (IC) chips, modules or substrates using capacitive coupling rather than conductive paths. For example, in large part, the need for multichip modules arises from the inability of the prior art to produce arbitrarily large semiconductor dies with acceptable yield as well as the high cost of wiring on semiconductor dies. Such problems have forced designers to partition large systems among multiple dies. To effect signalling between different chips and modules, the prior art requires the use of conductive connectors, solder bumps, wire-bond interconnections or the like. Unfortunately, such means introduces significant latency, frequency limitations and power requirements. To mitigate these problems, the present invention effects signalling capacitively. As described beginning at page 25, line 16, pairs of half-capacitor plates (Fig. 1, elements 13, 14), one half located on each IC chip (11), module or substrate (10), are used to capacitively couple signals from one IC chip, module or substrate to another. The use of such plates relaxes the area needed to effect signalling, and reduces or eliminates the requirements for exotic metallurgy.

(6) Issues

The claims have been rejected on several pieces of prior art in which capacitors are used to couple to ground power supply leads to an IC chip. Applicants submit that such references do not disclose or suggest their invention in which signal leads are capacitively coupled to an IC chip.

(7) Grouping of Claims

All the pending claims except claims 44 and 59 have been rejected as anticipated by or obvious over Moresco. These claims do not stand or fall together. Of these claims, claim 1 and claims 37-43, 45-48 and 52-58, which are dependent thereon, are believed to constitute one group of claims; and independent claims 28 and 102 and claims 143, 144, 146 and 147 which are dependent on claim 102 are believed to constitute a second group of claims that is separately patentable from the first group of claims.

(8) Argument

A. Hite, Dehaine et al. and Tanaka Do Not Anticipate Claim 1

Claim 1 of the present application recites:

1. A modular electronic system comprising:
 - a substrate;
 - a chip;
 - means for powering said chip;
 - means for capacitively signalling between said chip and said substrate; and
 - signal leads connected on said substrate and said chip to said means for capacitively signalling.

There is no dispute that the Hite reference discloses a substrate 2, a chip 10, a power supply lead 4, and a capacitor such as element 34. However, applicants take issue with the Examiner's assertion that elements 38 and 40 of Hite are signal leads. Lead 4 is identified at col. 4, lines 39-40 as being associated with either the positive power supply V_{cc} (col. 4, lines 39-40) or the ground, or reference power supply, V_{ss} (col. 4, lines 44-45). Hite states at column 5, lines 53-56, that wires 38 and 40 connect power supply lead 4 to chip 10:

"Bond wire 38 connects a lead 4 of header 2 to the top surface of capacitor 34, and bond wire 40 connects the top surface of capacitor 34 to a bond pad of chip 10".

Thus, it is evident that leads 38 and 40 are not signal leads but power supply leads.

There is also no dispute that the Dehaine et al. reference discloses a substrate 16, a chip 12, power supply leads 15a-13a; 15b-13b, capacitors 19, and signal input/output terminals 13s. Note, however, that Dehaine et al. is careful to distinguish the power supply leads 13a, 13b from the signal input/output terminals 13s at col. 3, lines 15-21:

The terminals 13 comprise signal input/output terminals 13s, and first and second supply terminals 13a, 13b intended to receive two different potentials, Va, Vb, respectively, for supplying the chip 12 with energy. For example, the potential Va represents ground and the potential Vb forms a voltage of +5 V with respect to ground.

There is also no dispute that Tanaka discloses a substrate 1 and a chip 5 and applicants are willing to concede that there must be a power supply lead to the chip but the specifics of how the chip is powered are not disclosed. Tanaka mentions that a pad 6 may be used to load a capacitor near semiconductor-chip loading region 2 but he does not depict a capacitor in his drawing and he does not disclose how it is used.

Contrary to the Examiner's assertions, however, the references applied do not disclose means for capacitively signalling between the chip and the substrate. This element of the claim is in means plus function format. In accordance with 35 U.S.C. § 112, paragraph 6, we must look to applicants' specification to determine the scope of this limitation. Fig. 1, for example, discloses:

"a means 13 for capacitively signalling, which provides a capacitive signal path between substrate 10 and die 11. Means 13 for capacitively signalling comprises two electromagnetically communicating regions illustratively depicted as 'half-capacitors' 14 and 15. A dielectric 17 is preferably used to partly or totally fill the gap between half-capacitors 14 and 15." Specification, p. 25, lines 21-25.

Similar such means are disclosed in many of the other figures.

As is evident from Fig. 2, the capacitive elements (identified as pairs of half-capacitors 13) are located in the signal path between leads on substrate 10 such as transmission lines 32 and 33 and leads on die 10 such as transmission lines 34 and 37. Further, as shown in Fig. 3, the capacitive interconnection between die and substrate shown to the left of the figure is different from a series of conductive connections means 41, 42, 43 shown to the right of the figure. In page 33, lines 16-21 it is noted that conductive contact

pads on die 11 "illustratively receive power, ground and a plurality of I/O signals from substrate 10" via connection means 41, 42, 43. Thus, a careful distinction is drawn in applicants' specification between signalling leads and power supply leads.

To the extent that the references describe the use of capacitors, the capacitors are used in power supply circuits not signalling circuits. Dehaine et al. goes to some length at col. 1, lines 20-27, to distinguish between signalling leads and power supply leads:

Among the input/output terminals of the package, the signal terminals are distinguished from the supply terminals intended for receiving various predetermined external electrical potentials. Similarly, in the interconnect structure, the signal conductors are distinguished from the supply conductors, which serve to route the supply potentials to the integrated circuit.

And he further explains at col. 1, lines 28-36 that it is customary to connect a capacitor to the supply conductors to reduce reactance.

A package for a VLSI chip must meet very stringent conditions. On the one hand, the reactive component of the supply conductors must be reduced to a minimum. This is ordinarily done by a decoupling device incorporated in the package. The decoupling device ordinarily includes conductor faces, which are connected to the plates of at least one decoupling capacitor and respectively receive the various potentials applied to the supply terminals of the package.

Dehaine goes on to disclose a circuit in which first and second voltage supply terminals 13a and 13b receive two different potentials V_a , V_b to supply energy to chip 12 (col. 3, lines 16-19). The potentials V_a , V_b are also supplied to groups 15a, 15b of supply terminals 15 and to conductor faces 18a, 18b and the plates of four decoupling capacitors 19 (col. 3, lines 23-25, 30-32). The voltage supply terminals are distinguished from the signal input/output terminals 13s (col. 3, lines 15 and 16) and the signal terminals 14 (col. 3, line 23). Of particular importance to the present discussion, while Dehaine discloses a connection between the voltage supply circuitry and capacitors 19, he does not disclose any connection between the signal terminals and a capacitor and, in particular, does not disclose a capacitive coupling in the signal lead between the substrate and the die.

Similarly, Hite does not disclose a capacitor in the signal lead between the substrate and the die. As is apparent from Figs. 2 and 5, the capacitors disclosed in Hite (elements 14 and 16 of Fig. 2 and elements 34, 35, 46 and 48 of Fig. 5) are used in power supply circuits between the V_{cc} , V_{bb} and V_{ss} power supply leads and are not used in signal leads at all.

As for Tanaka, he does not illustrate a specific circuit that uses a capacitor and does not describe how the capacitor is used. In the absence of any specific disclosure, Tanaka cannot be said to disclose the use of a coupling capacitor in a signal line between the substrate and the chip.

Because none of these references discloses means for capacitively signalling between chip and substrate, they likewise do not disclose signal leads on the chip and substrate that are connected to such means.

For the foregoing reasons, it is submitted that the rejection of claim 1 under 35 U.S.C. 102(b) as anticipated by Hite, Dehaine and Tanaka is in error and should be withdrawn.

B. Moresco et al. Does Not Anticipate or Suggest Claim 1 or the Claims Dependent Thereon

Again, there is no dispute that Moresco et al. discloses a substrate 20 and a chip 10 and applicants note that the Moresco's purpose is to provide a relatively noise free source of power (col. 1, line 23) by forming a power supply by-pass capacitor that is close to the IC chip (col. 2, lines 24-26).

Moresco, however, does not disclose or suggest the use of a means for capacitively signalling between the chip and substrate. Rather, Moresco carefully distinguishes between signal line connections and power connections. He states:

Various methods are available for connecting IC chips to other devices. Connections are required not only for power supply, but also for signal lines between chips, other device components and various input/output ("I/O") devices. Col. 1, lines 45-49.

And, in forming his by-pass capacitor, Moresco explains that he uses solder bumps "that are not needed for signal or power conduction" (col. 3, lines 59-60).

Further, Moresco explains that his by-pass capacitor is connected between a power supply line and ground.

"Again, one of these plates [of the bypass capacitor] must be electrically connected to ground while the other is connected to the power supply line."

Since a power supply line is not a signal line and was carefully distinguished from a signal line in both Moresco's patent and in applicants' specification, Moresco's teaching

cannot be said to disclose or suggest the claimed means for capacitively signalling between a chip and a substrate. For the same reason, Moresco also does not disclose signal leads on the substrate and chip that are connected to the means for capacitively signalling.

Accordingly, claim 1 is believed to be patentable over Moresco.

The claims dependent on claim 1 are believed patentable for the same reason claim 1 is patentable.

C. Moresco et al. Does Not Anticipate or Suggest Claims 28, 102, 143 144, 146 and 147

Claim 28 of the present application recites:

28. An electronic system comprising:
a chip;
a substrate;
a plurality of electronic devices implemented on said chip, a signal lead of at least one of said plurality of electronic devices coupled to a first half-capacitor attached to said chip; and,
a second half-capacitor attached to said substrate and capacitively coupling a signal to said first half-capacitor.

Claim 28 explicitly recites first and second half-capacitors attached to the chip and substrate with a signal lead connected to the first half-capacitor and the second half-capacitor capacitively coupling a signal to the first half-capacitor. It is patentably distinct from claim 1 because it does not recite in means plus function language means for capacitively signalling between chip and substrate.

As emphasized above, Moresco discloses a by-pass capacitor for capacitively connecting a power supply line to ground (col. 6, lines 27-29). Moresco uses this circuit to deliver a relatively noise free power source to the IC chip. This, however, does not disclose or suggest capacitively coupling a signal between chip and substrate using half-capacitors as claimed in claim 28.

For this reason, claim 28 is believed to be patentable over Moresco.

Similarly, claim 102 recites first and second modules having half-capacitors with a plurality of electronic devices connected to the first half-capacitor and a capacitive signal path between the first and second modules:

102. A modular electronic system comprising:
a first module having a plurality of electronic devices, a first half-capacitor and at least one signal lead connecting said electronic devices to said first half-capacitor; and
a second module having a second half-capacitor, said modules being positioned such that said first and second half-capacitors provide a capacitive signal path between said first and second modules.

Again, Moresco fails to disclose or suggest the use of capacitive coupling of signals between two modules because his by-pass capacitor merely couples a power supply line to ground.

For this reason, claim 102 and dependent claims 143, 144, 146 and 147 are believed to be patentable over Moresco.

(9) Appendix - Claims on Appeal

1. A modular electronic system comprising:
a substrate;
a chip;
means for powering said chip;
means for capacitively signalling between said chip and said substrate; and
signal leads connected on said substrate and said chip to said means for capacitively signalling.
28. An electronic system comprising:
a chip;
a substrate;
a plurality of electronic devices implemented on said chip, a signal lead of at least one of said plurality of electronic devices coupled to a first half-capacitor attached to said chip; and,
a second half-capacitor attached to said substrate and capacitively coupling a signal to said first half-capacitor.
37. A modular electronic system as defined in claim 1 wherein the capacitance of said means for capacitively signaling is selected to provide a high bandwidth connection to a transmission line.

38. A modular electronic system as defined in claim 1 wherein said means for capacitively signaling is adapted to have substantially lower parasitic inductance than would a conductive connection adapted for the same total use of chip area.

39. A modular electronic system as defined in claim 1 wherein said means for capacitively signaling comprises first and second coupled half-capacitors, said first half-capacitor being associated with said chip and said second half-capacitor being associated with said substrate, said first and second coupled half-capacitors comprising substantially overlapping conductive regions separated by a gap.

40. A modular electronic system as defined in claim 39 wherein at least one of said conductive regions comprises a plate.

41. A modular electronic system as defined in claim 39 wherein the capacitance of said means for capacitively signaling can be varied by changing the effective area of overlap between said conductive regions.

42. A modular electronic system as defined in claim 39 wherein portions of said chip are passivated, but not said first half-capacitor.

43. A modular electronic system as defined in claim 39 wherein said gap is at least partially filled with a dielectric.

44. A modular electronic system comprising:
a substrate;
a chip;
means for powering said chip;
means for capacitively signaling between said chips and said substrate
comprising first and second coupled half-capacitors, said first half-capacitor being associated with said chip and said second half-capacitor being associated with said substrate, said first and second coupled half-capacitors comprising effectively

overlapping conductive regions separated by a gap that is at least partially filled with a dielectric; and

a power connector extending through said dielectric.

45. A modular electronic system as defined in claim 43 wherein said dielectric accommodates mechanical guides.

46. A modular electronic system as defined in claim 43 further comprising a power connection extending through said dielectric.

47. A modular electronic system as defined in claim 43 further including passivation distinct from said dielectric.

48. A modular electronic system as defined in claim 47 wherein said dielectric has a substantially greater dielectric factor than does said passivation.

52. A modular electronic system as defined in claim 1 wherein said means for capacitively signaling operates despite a substantial misalignment between said substrate and said chip.

53. A modular electronic system as defined in claim 39 further comprising a plurality of coupled half-capacitors, a substantial area of said chip and a substantial portion of the area of said substrate overlapping said chip being covered with substantially overlapping half-capacitors.

54. A modular electronic system as defined in claim 53 wherein at least one half-capacitor on said chip is connected to a chip ground, power, or other common reference signal.

55. A modular electronic system as defined in claim 53 wherein at least one half-capacitor on said substrate is connected to a substrate ground, power, or other common reference signal.

56. A modular electronic system as defined in claim 39 wherein the area of one of said conductive regions is greater than the area of the other of said conductive regions.

57. A modular electronic system as defined in claim 39 wherein the shape of one of said conductive regions differs from the shape of the other of said conductive regions.

58. A modular electronic system as defined in claim 39 wherein said first half-capacitor overlays circuitry.

59. A modular electronic system comprising:
a substrate;
a chip;
means for powering said chip;
means for capacitively signaling between said chips and said substrate
comprising first and second coupled half-capacitors, said first half-capacitor being associated with said chip and said second half-capacitor being associated with said substrate, said first and second coupled half-capacitors comprising effectively overlapping conductive regions separated by a gap; and
an additional half-capacitor on its backside.

102. A modular electronic system comprising:
a first module having a plurality of electronic devices, a first half-capacitor and at least one signal lead connecting said electronic devices to said first half-capacitor;
and
a second module having a second half-capacitor, said modules being positioned such that said first and second half-capacitors provide a capacitive signal path between said first and second modules.

143. A modular electronic system as defined in claim 102 wherein said first and second half-capacitors are shaped such that the admittance of said capacitive signal path is substantially unaffected by a small misalignment between said first and second modules.

144. A modular electronic system as defined in claim 102 wherein the area of one of said half-capacitors is greater than the area of the other of said half-capacitors.


146. A modular electronic system as defined in claim 102 wherein the shape of one of said half-capacitors differs from the shape of the other half-capacitor.

147. A modular electronic system as defined in claim 146 wherein said shape of said one of said half-capacitors is designed to accommodate anticipated misalignment.

For the foregoing reasons, the claims on appeal are believed to be patentable and in condition for allowance. Such action is respectfully requested.

Respectfully Submitted,

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Francis E. Morris Reg. No. 24,615
PENNIE & EDMONDS LLP
1155 Avenue of the Americas
New York, NY 10036-2711
(650) 493-4935